

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (currently amended) A control circuit for controlling an output voltage of a DC/DC converter, wherein the DC/DC converter includes a main switching element and a synchronous switching element, the control circuit comprising:

a pulse signal generation circuit which generates a pulse signal for controlling the output voltage of the DC/DC converter based on the output voltage; and

a drive signal generation circuit connected to the pulse signal generation circuit in which the drive signal generation circuit generates first and second drive signals using the pulse signal for respective supply to the main switching element and the synchronous switching element such that the main switching element and the synchronous switching element are turned ON and OFF alternately at different timings as a result of receiving the first and second drive signals, and the drive signal generation circuit generates the first drive signal such that the first drive signal has the same pulse width as that of the pulse signal,

wherein the drive signal generation circuit generates the second drive signal having a pulse width greater than that of the first drive signal when the first drive signal is supplied to the main switching element, and

wherein the drive signal generation circuit includes:
a first delay circuit which generates the first drive signal by delaying the pulse signal;
a second delay circuit connected to the first delay circuit, the second delay circuit
generating a delayed signal by delaying the first drive signal; and
a synthesis circuit connected to the second delay circuit, and the synthesis circuit
generating the second drive signal by synthesizing the pulse signal with the delayed signal.

Claim 2 (original) The control circuit according to claim 1, wherein the drive signal generation circuit generates the second drive signal such that the second drive signal has a larger pulse width than the first drive signal using the pulse signal and the first drive signal.

Claim 3 (canceled).

Claim 4 (currently amended) The control circuit according to claim 1 [[3]], wherein the first and second delay circuits each ~~include~~ includes a plurality of inverter circuits.

Claim 5 (currently amended) The control circuit according to claim 1 [[3]], wherein the first and second delay circuits each ~~include~~ includes an integrating circuit having a resistor and a capacitor.

Claim 6 (currently amended) The control circuit according to claim 1 [[3]], wherein the synthesis circuit includes a NOR circuit.

Claim 7 (currently amended) A control circuit for controlling an output voltage of a DC/DC converter, wherein the DC/DC converter includes a main switching element and a synchronous switching element, the control circuit comprising:

an error amplification circuit which compares the output voltage of the DC/DC converter and a reference voltage to generate an error signal;

a comparison circuit connected to the error amplification circuit in which the comparison circuit compares the error signal and a triangular wave signal to generate a pulse signal having a pulse width proportional to the voltage of the error signal; and

a drive signal generation circuit connected to the comparison circuit, the drive signal generation circuit generating first and second drive signals using the pulse signal for respective supply to the main switching element and the synchronous switching element such that the main switching element and the synchronous switching element are turned ON and OFF alternately at different timings due to receiving the first and second drive signals, and the drive signal generation circuit generating the first drive signal such that the first drive signal has the same pulse width as that of the pulse signal,

wherein the drive signal generation circuit generates the second drive signal having a pulse width greater than that of the first drive signal when the first drive signal is supplied to the

main switching element, and

wherein the drive signal generation circuit includes:

a first delay circuit which generates the first drive signal by delaying the pulse signal;

a second delay circuit connected to the first delay circuit, the second delay circuit
generating a delayed signal by delaying the first drive signal; and

a synthesis circuit connected to the second delay circuit, the synthesis circuit generating
the second drive signal by synthesizing the pulse signal with the delayed signal.

Claim 8 (original) The control circuit according to claim 7, wherein the drive signal generation circuit generates the first drive signal by delaying rising and falling of the pulse signal.

Claim 9 (original) The control circuit according to claim 7, wherein the drive signal generation circuit generates a delayed signal by delaying rising and falling of the first drive signal and generates the second drive signal by synthesizing the delayed signal with the pulse signal.

Claim 10 (canceled) .

Claim 11 (currently amended) The control circuit according to claim 7 [[10]], wherein the first and second delay circuits each ~~include~~ includes a plurality of inverter circuits.

Claim 12 (currently amended) The control circuit according to claim 7 [[10]], wherein the first and second delay circuits each ~~include~~ includes an integrating circuit having a resistor and a capacitor.

Claim 13 (currently amended) The control circuit according to claim 7 [[10]], wherein the synthesis circuit includes a NOR circuit.

Claim 14 (currently amended) A DC/DC converter comprising:
a main switching element;
a synchronous switching element connected in series to the main switching element;
a smoothing circuit connected to a node between the main switching element and the synchronous switching element, the smoothing circuit generating an output voltage; and
a control circuit which controls the output voltage by supplying a first drive signal to the main switching element and supplying a second drive signal to the synchronous switching element, the control circuit including:

a pulse signal generation circuit which generates a pulse signal for controlling the output voltage based on the output voltage; and

a drive signal generation circuit connected to the pulse signal generation circuit, the drive signal generation circuit generating the first and second drive signals by using the pulse signal such that the main switching element and the synchronous switching element are turned ON and

OFF alternately at different timings, and the drive signal generation circuit generating the first drive signal such that the first drive signal has the same pulse width as that of the pulse signal, wherein the drive signal generation circuit generates the second drive signal having a pulse width greater than that of the first drive signal when the first drive signal is supplied to the main switching element, and

wherein the drive signal generation circuit includes:

a first delay circuit which generates the first drive signal by delaying the pulse signal;

a second delay circuit connected to the first delay circuit, the second delay circuit generating a delayed signal by delaying the first drive signal; and

a synthesis circuit connected to the second delay circuit, the synthesis circuit generating the second drive signal by synthesizing the pulse signal with the delayed signal.

Claim 15 (original) The DC/DC converter according to claim 14, wherein the drive signal generation circuit generates the second drive signal having a larger pulse width than the first drive signal using the pulse signal and the first drive signal.

Claim 16 (original) The DC/DC converter according to claim 14, wherein the drive signal generation circuit includes:

a first delay circuit which generates the first drive signal by delaying the pulse signal;

a second delay circuit connected to the first delay circuit, the second delay circuit

generating a delayed signal by delaying the first drive signal; and

a synthesis circuit connected to the second delay circuit, and the synthesis circuit generating the second drive signal by synthesizing the pulse signal and the delayed signal.

Claim 17 (currently amended) The DC/DC converter according to claim 16, wherein the first and second delay circuits each ~~include~~ includes a plurality of inverter circuits.

Claim 18 (currently amended) The DC/DC converter according to claim 14 [[16]], wherein the first and second delay circuits each include an integrating circuit which having a resistor and a capacitor.

Claim 19 (currently amended) The DC/DC converter according to claim 14 [[16]], wherein the synthesis circuit includes a NOR circuit.

Claim 20 (currently amended) The DC/DC converter according to claim 14 [[16]], wherein the pulse signal generation circuit includes:

an error amplification circuit which compares the output voltage and a reference voltage to generate an error signal; and

a comparison circuit connected to the error amplification circuit, and the comparison circuit comparing the error signal and a triangular wave signal to generate a pulse signal having a

pulse width proportional to the voltage of the error signal.

Claim 21 (currently amended) A method for controlling an output voltage of a DC/DC converter, wherein the DC/DC converter includes a main switching element and a synchronous switching element, the method comprising:

generating a pulse signal for controlling the output voltage of the DC/DC converter based on the output voltage;

generating a first drive signal which has the same pulse width as that of the pulse signal by delaying the pulse signal and supplying the first drive signal to the main switching element;
[[and]]

generating a delayed signal by delaying the first drive signal; and

generating a second drive signal ~~using the pulse signal and the first drive signal by synthesizing the pulse signal and the delayed signal~~ and supplying the second drive signal to the synchronous switching element such that the main switching element and the synchronous switching element are turned ON and OFF alternately at different timings and the second drive signal has a pulse width greater than that of the first drive signal when the first drive signal is supplied to the main switching element.